Co-designed electro-optical integrated frontend circuits for high speed transceivers

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Abstract: *Co-design of photonic and electronic chips has become a necessity to realize high-performance transceivers. This paper will illustrate a number of recent developments of high-speed transceiver circuits including broadband driver amplifiers and transimpedance amplifiers.*
Keywords: *optical transceiver, optical interconnect, driver, transimpedance amplifier*

I. INTRODUCTION

New circuit architectures and technologies for high-speed electronic and photonic integrated circuits are essential to realize optical interconnects with higher symbol rate to follow the increasing demand of data intensive applications such as cloud services, virtual reality, high-performance computing, 5G/6G, etc. pushing the speeds of all sorts of interconnects and interfaces. Progress on transceiver throughput typically comes from technology evolutions and smarter integrated circuit (IC) and system design. Smarter design concerns the invention and realization of new circuits and architectures, more efficient multiplexing or modulation schemes, digital signal processing, etc. Due to the increasing speeds and multi-channel operation, the design and verification process becomes increasingly complex and challenging considering signal integrity, power integrity, process variations, design rules, thermal and packaging aspects etc. Besides creativity and accumulated design expertise, advancements in technology are crucial as enabling factor. This involves for example new electro-optic materials and devices (e.g. based on graphene or plasmonics), hybrid integration through new assembly techniques such as transfer printing of chiplets, and advancement of CMOS and SiGe BiCMOS technologies.

From a high-speed analog design perspective SiGe BiCMOS provides several advantages compared to CMOS such as higher f_T, higher break down voltage, higher drive current/voltage, higher transconductance and intrinsic gain, lower noise, better metal stacks for high-Q passives and interconnects and more intuitive/traditional circuit design [1]. However, the integration density is limited by the relatively large CMOS node (55nm, 90nm,…) which limits mixed-signal and digital signal processing (DSP) capabilities. Today's mainstream CMOS technologies on the other hand allow integrating huge amounts of transistors with densities on the order of 100 million per square mm. Enormous investments, technology development and new transistor concepts are fueling the continued scaling in next generation CMOS processes. This economic reality makes that if a circuit can be implemented in CMOS, it will be most likely done in CMOS, but high product volumes are needed. The ongoing CMOS scaling increases the digital circuit performance, enabling the extensive usage of DSP, calibration, predistortion and equalization. For analog circuits, the CMOS sweetspot is roughly around 28nm, beyond which the f_T drops each new generation due to increased parasitic capacitance in the transistor structure [2].

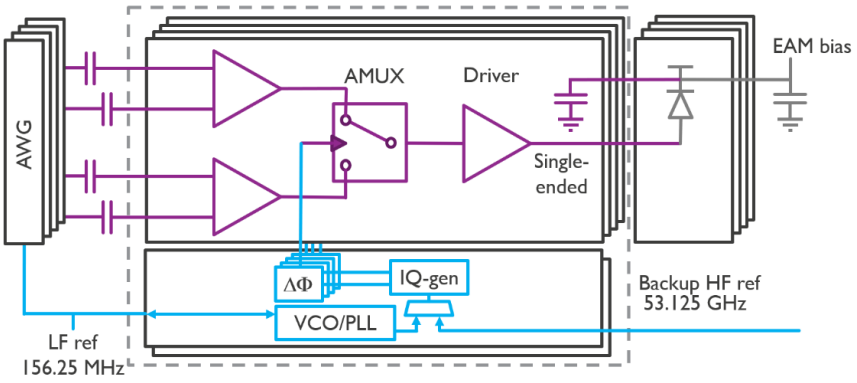

Figure 1. Quad channel 106 Gbaud 2-to-1 MUX with modulator driver, VCO/PLL clock generator and clock tree. In this configuration a single-ended electro-absorption modulator (EAM) is considered.

The remainder of this paper will focus on our most recent developments of quad-channel modulator driver and transimpedance amplifier chips at 100-120 Gbaud in SiGe BiCMOS. However, our ongoing research and development is increasingly using finfet CMOS for feasibility studies and proof-of-concept designs for e.g. 112 Gbaud DSP-based clock-and-data recovery (CDR) and high-sampling rate digital-to-analog-converters (DACs), complementing imec's research on analog-to-digital converters (ADCs). Test results of other chips at 100-120 Gbaud can be found in [3] and [4] where our research focused on analog interleaving and multiplexing in combination with a compact 7-tap mixed-signal Feed-Forward Equalizer in 55nm SiGe BiCMOS.

II. QUAD-CHANNEL 106 GBAUD 2:1 LINEAR MULTIPLEXER WITH INTEGRATED MODULATOR DRIVER AND INTEGRATED PLL/VCO

To scale up throughput to 800Gb/s, a fully integrated quad-channel SiGe BiCMOS transmitter front-end is being developed in H2020 Poetics, shown in Figure 1. The main functionality in each channel of the transmit path consists of a 2:1 analog signal multiplexer (AMUX) and a high-bandwidth linear driver DRV, referred to together as AMUX-DRV. The AMUX interleaves two incoming PAM-4 signals to generate a PAM-4 signal at twice the symbol rate. The AMUX operation requires a 53 GHz clock synchronized with the incoming 53 Gbaud PAM-4 data to alternate between the two data inputs, with very low jitter, as jitter reduces the SNR. For this purpose, an on-chip voltage controlled oscillator (VCO) and phase-locked-loop (PLL) is integrated, which can be locked to an external frequency reference and which can provide a phase controlled clock for each channel. The 2:1 106GBaud AMUX will be based on return-to-zero pulse shaping and interleaving, similar to the analog interleaver of [3]. The output stage can be reconfigured for single-ended or differential operation, and the 50 Ohm back-termination resistors can be disconnected with a Focused Ion Beam (FIB). Figure 2 gives a view on the floorplan of the quad AMUX-DRV chip in 90 nm SiGe BiCMOS. Fabrication is currently ongoing.

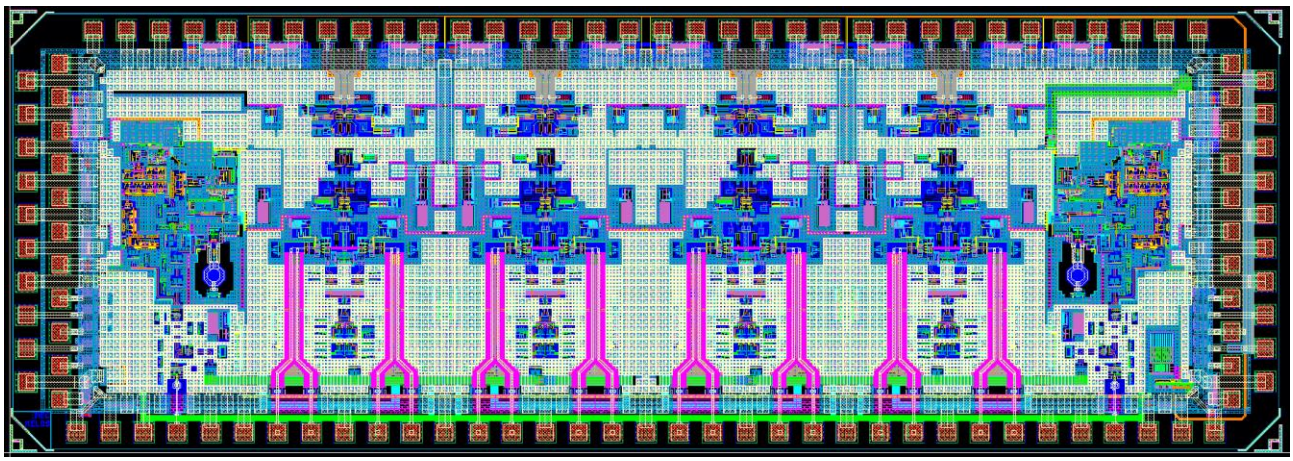

Figure 2. Quad channel 106 Gbaud 2-to-1 MUX with modulator driver and clock generator

III. 106 GBAUD QUAD-CHANNEL TIA AND MZM DRIVER

Figure 3 and Figure 4 show a quad-channel TIA and MZM driver chip, both designed in 55nm SiGe BiCMOS, fabrication finished at the moment of writing.

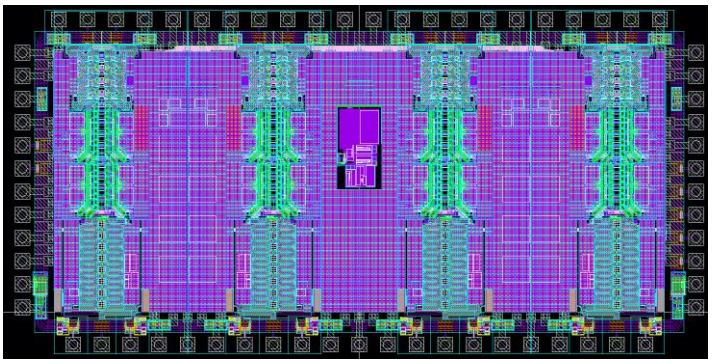

Figure 3. Quad channel 106 Gbaud TIA

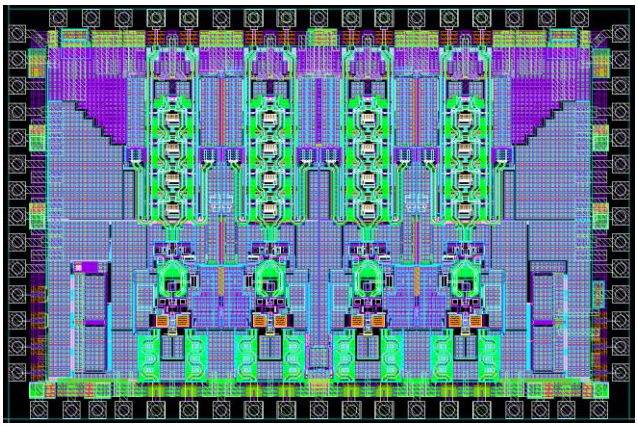

Figure 4. Quad channel 106 Gbaud MZM driver

The quad-channel linear TIA array is designed for a bandwidth of 50 to 60GHz, and low total harmonic distortion (THD) below 5% for an output swing of 0.5Vpp. The PAM-4 optical modulation amplitude (OMA) sensitivity is estimated to be around minus 6 dBm (without intersymbol interference penalty and considering a target BER of 10^{-4}). The TIA input stage is suitable for both single and balanced photodiodes. The power consumption is expected to be around 500 mW per channel. The quad-channel linear MZM driver is co-designed with a Silicon Photonic dual-polarization IQ modulator and targeted a bandwidth of 80-90 GHz, with a differential output swing of 2 to 2.5 Vpp. The MZM driver power consumption will be somewhat below 700 mW per channel.

IV. CONCLUSIONS

This invited paper presented a number of (ongoing) 100-120 Gbaud circuit developments for next-generation high-speed optical transceivers. To further scale the capacity of optical transceivers to a next level, ongoing research is exploring various ways forward for which custom high-speed electronics remains a crucial part in the development. For sure, technology, circuit topologies, design techniques, and co-integration methods will progress in the coming years. In this respect, high-speed optical interconnects will benefit from several other applications pushing transceiver operation towards higher frequencies, such as 6G, radar, sub-THz etc. Novel high-mobility semiconductor materials and transistor concepts are being developed to enhance performance and sustain the scaling of transistor technology. As an alternative, hybrid integration through advanced packaging such as transfer printing (H2020 Caladan) allows to mix and match small electronic and/or photonic chiplets with much lower parasitics than conventional flip-chip assembly. Furthermore, progress can be expected from the evolution of circuit architecture and design tools, and new transceiver concepts combining electronic and photonic ICs (electro-optical DACs, optical equalization, optical time division multiplexing, optical sampling…). However, the R&D on this road is a huge challenge and investment with an increasing list of issues/risks to be tackled. For example, power consumption is certainly a big concern for signal generation, and the clock generation and distribution in particular [5]. Nevertheless, a very exciting decade lies ahead for R&D on high-capacity links and transceivers with symbol rates beyond 100 Gbaud in both direct detect and coherent systems.

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