Electronic and photonic IC co-design for high-speed optical transceivers

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New circuit architectures and technologies for high-speed electronic and photonic integrated circuits are essential to realize optical interconnects with higher symbol rate. As a consequence of the increasing speeds, close integration and co-design of photonic and electronic chips have become a necessity to realize high-performance transceivers with novel packaging approaches.

This presentation will illustrate a number of recent developments of application-specific high-speed electro-optic transceiver circuits including e.g. broadband driver amplifiers, multiplexer circuits and transimpedance amplifiers for signal generation and reception at 100 Gbaud and beyond. Fig. 1 shows such a recent example of a highly integrated SiGe BiCMOS chip including a quad channel 106 Gbaud 2-to-1 analog multiplexer with a reconfigurable modulator driver (supporting both differential and single-ended operation, and with removable internal back-terminations) and including a 53 GHz clock generator (phase-locked loop, PLL; voltage controlled oscillator, VCO). The basic concepts and architectures, technological aspects, design challenges and trade-offs will be discussed.

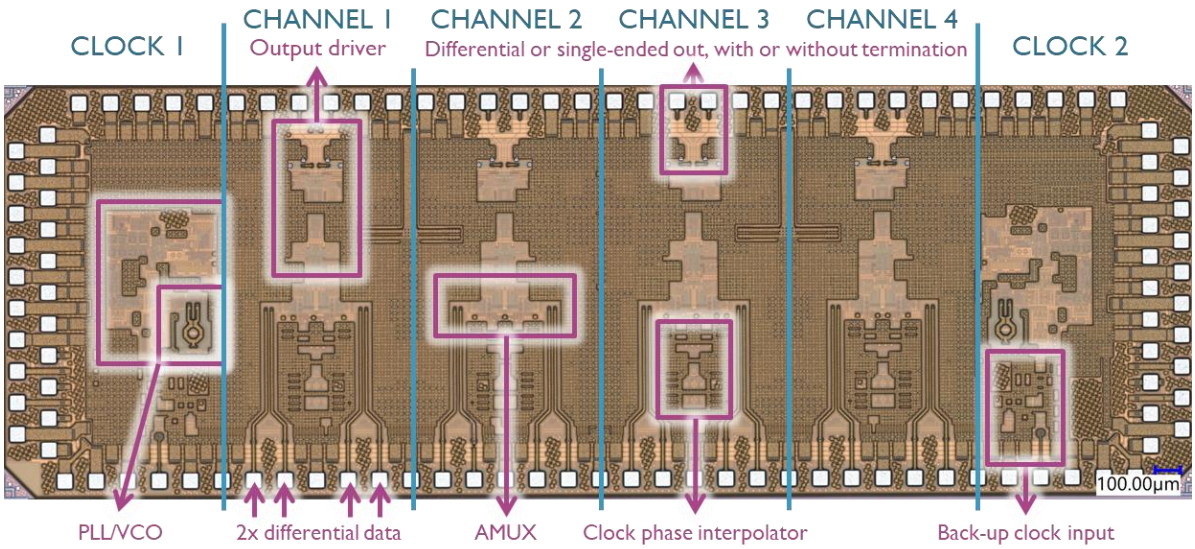

Fig. 1: Micrograph of a quad channel 106 Gbaud 2-to-1 analog multiplexer with reconfigurable modulator driver, VCO/PLL clock generator and clock tree

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