

# Hybrid integration of Polymer PICs and InP optoelectronics for WDM and SDM terabit intra-DC optical interconnects

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**Abstract**— This paper presents a hybrid photonic integration concept based on the use of a polymer motherboard, InP EML arrays and InP PD arrays to realize WDM and SDM Terabit optical engines operating at 100-Gb/s or even at 200-Gb/s per lane. The optical engines are aligned with the Ethernet roadmap, are cost-efficient by design and can find their place in the next generation Terabit IM/DD optical transceivers within Data Centers.

**Keywords**—hybrid photonic integration, EMLs, polymer PICs, optical transceivers, GbE

## I. INTRODUCTION

The ever-growing bandwidth requirements are pushing the developments for the next generation terabit optical transceivers. The paths towards increasing the optical transceiver capacity are by either increasing the serial speed of the transceiver's components [1],[2] or increasing the number of lanes [3]. Currently serial speeds are approaching 200-Gb/s per lane, nonetheless still the whole transceiver requires many lanes, and thus fibers, to reach 1.6T capacity. Deploying more optical fibers inside datacenters (DCs) to accommodate the capacity increase might not be as cost-efficient. Wavelength division multiplexing (WDM) optical

transceivers can alleviate this problem, but it is not unlikely that DC operators will turn to the deployment of multi-core fibers (MCFs) inside DCs to cope with the capacity increase [4]. When operated in parallel single mode (PSM), the MCFs allow for uncooled operation of the optical engine, while if combined with WDM can provide tremendous capacity increase. In this paper, we present hybrid photonic integration concepts for realizing WDM and spatial division multiplexing (SDM) Terabit optical engines, sharing the same fundamental building blocks. The concept is based on the edge-coupling of InP electroabsorption-modulated laser (EML) and photodiode (PD) arrays, for minimizing the number of components and interfaces, with a polymer photonic integrated circuit (PIC) motherboard having the required toolbox for WDM and SDM functionality, such as multi-channel arrayed waveguide gratings (AWGs) and 3D waveguide layers for interfacing to MCFs. The use cases are given in Section II, while the WDM and SDM optical engine concepts are given in Sections III and IV. The paper concludes in Section V.

## II. USE CASES AND APPLICATION

DCs are constantly evolving pushed by new services and application requirements [5] and a continuous effort toward sustainability (surpass of digital divide, power consumption reduction, search for reusable and sustainable materials) [6]. To that end, new trends in DC concept have been proposed:

- edge DCs, located close to the network's edge, asking for high capacity in a smaller footprint, fast services provisioning and reconfiguration, minimal latency.
- central offices re-architected as DCs, capitalizing on the benefits of network function virtualization, software defined networks, and open-source software, asking for the technology readiness level and the reliability of telco services and for coexistence with legacy infrastructure.
- massive introduction of automation and predictive analysis to cope with data-hungry technologies and enable the development of data-generating artificial intelligence or machine learning.

## III. WDM OPTICAL ENGINES

### A. InP EML arrays and PD arrays

For the Tx side, 4-fold and 8-fold InP EML array batches having 400 GHz spacing in the frequency grid, covering the ranges 1273 – 1291-nm, 1293 – 1309-nm have been fabricated. The EMLs exhibited modulation bandwidth >35-GHz, capable of 53-GBaud 4-level pulse amplitude modulation (PAM-4) operation, output power ex. facet >20-mW, employing an integrated semiconductor optical amplifier (SOA) on the same die, and static extinction ratio >10-dB while driven at moderate injection current values for the distributed feedback laser (DFB) and SOA sections. For the Rx side, 4-fold and 8-fold waveguide integrated PD arrays have been fabricated at HHI's InP technology. The PDs exhibited 50-GHz bandwidth, 0.6-A/W responsivity with practically no polarization dependence across the O-band.

### B. Polymer motherboards for wavelength (de)multiplexing

The wavelength demultiplexing functionalities of the optical engine are realized by means of 8-ch and 16-ch AWGs designed and fabricated on the PolyBoard platform. PolyBoard makes an ideal photonic motherboard due to its ease of fabrication and thus lower cost compared to other

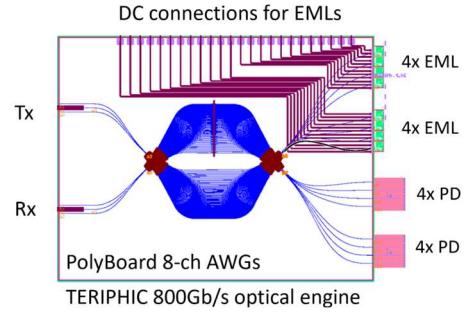


Figure 1. PolyBoard motherboard hosting 8-ch AWGs for the 800Gb/s optical engine.

materials, and low-loss edge-coupling of the InP elements. A schematic of such 8-ch AWGs is shown in Fig.1. A half-wave plate inserted in the middle of the demux AWG ensures polarization independence. The insertion losses for the 8-ch AWGs are <5-dB. The channel spacing is 400-GHz exhibiting crosstalk of <-20-dB. The 1.6T optical engine is a direct extension of the 800G, having two 8-fold EML and PD arrays.

### C. Hybridly integrated terabit optical engines

The hybridly integrated 800Gb/s optical engine can be seen in Fig. 2. The 4x EML and 4x PD arrays are edge-coupled to the PolyBoard motherboard with <2.0-dB and <1.5-dB loss, respectively. The DFB and SOA sections are wirebonded on the DC traces of the DC interposer so that appropriate voltage signals can be applied. The ground-signal-ground pads of the EML and PD arrays are at the back of the optical engine to facilitate interconnection with the EML drivers and transimpedance amplifiers. U-grooves at the Tx and Rx sides of the PolyBoard facilitate low-loss (<1.6-dB) fiber-pigtailing with standard single-mode fiber pigtails. The assembly of the EML/PD arrays as well as the fiber pigtail processes for these optical engines has been automated in the framework of TERIPHIC project [7].

## IV. SDM OPTICAL ENGINES

The same fundamental technology was used in POETICS

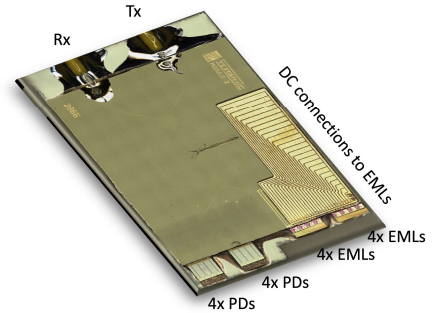


Figure 2. Photograph of 800Gb/s optical engine. The DC interposer for EML DC supplies can be seen on the right.

project to develop co-packaged optical engines with up to 1.6T capacity, keeping the same lane number (8), but doubling the symbol rate to 100-GBaud to achieve 200-Gb/s per lane. SDM was selected because it can provide the capacity upgrade that will soon be needed inside the DC networks and also allows for PSM transmission and thus uncooled operation of the EMLs which consequently reduces power consumption.

### A. Uncooled InP EML arrays and PD arrays

For the Tx side, the EML technology was upgraded to achieve higher bandwidth using a single multi-quantum well

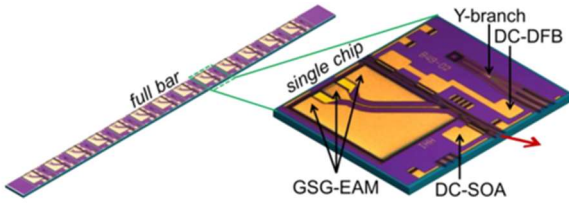


Figure 3. Photograph of fabricated EML array.

layer stack design making it more cost-efficient. Using this technology 4-fold arrays with  $>50$ -GHz bandwidth over a temperature range of  $20$ - $85^{\circ}\text{C}$ , and optical output power of  $10$ -dBm (thanks to the integrated SOA) have been fabricated [8]. Fig.3 shows such a device. The Y-branch was added to facilitate hybrid integration using optical alignment loops on the PolyBoard. The same PD technology described in Section II is used at the Rx side as it has the required bandwidth for 100-GBaud PAM-4 operation.

### B. Polymer motherboards for SDM

Key enablers for the development of the SDM terabit optical engine, are the multi-layer PolyBoard platform [9] and the 3D multi-mode interference structure [10] that allows transitions between the waveguide layers with  $<2.5$ -dB loss. In more detail, PolyBoard was fabricated to have 3 waveguide layers, with the two outer (first and third) layers having arrays of 4 waveguides, arranged to match the  $2 \times 4$  waveguide pattern of the MCFs. Each layer has a height of approx.  $17\text{-}\mu\text{m}$ , thus

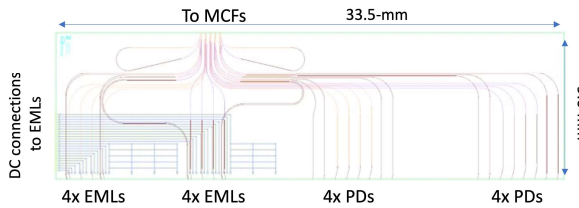


Figure 4. 3D PolyBoard motherboard mask layout showing the interfaces to the EML arrays and the PD arrays.

covering the vertical MCF core distance with 3 layers. The 3D PolyBoard motherboard measures  $3.35$  cm in length and  $9.6$  mm in width. One 8-core MCF is used per direction (Tx, Rx), plus additional MCFs that interface alignment waveguides. The MCF core pitch is  $35\text{-}\mu\text{m}$  at the horizontal and  $45\text{-}\mu\text{m}$  at the vertical directions. The mode-field diameter (MFD) is  $8.6\text{-}\mu\text{m}$ , which closely matches PolyBoard's channel waveguide MFD, ensuring efficient coupling.

### C. Hybridly integrated optical engines

The 3D PolyBoard motherboard schematic can be seen in Fig. 5. The EML and PD arrays are hybridly integrated by

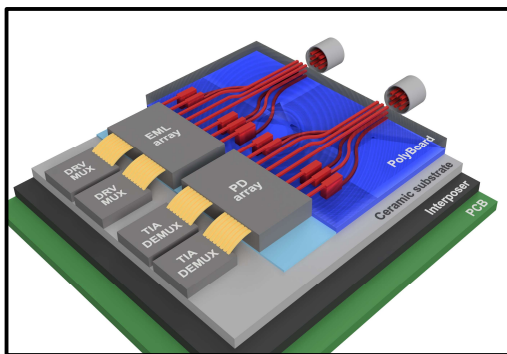


Figure 5. Schematic of POETICS SDM 1.6T optical transceiver.

means of edge-coupling with  $<2.0$ -dB and  $<1.5$ -dB coupling loss per waveguide, respectively. DC connections to the EMLs are realized by means of DC tracks directly fabricated on the PolyBoard motherboard itself and not by means of a DC interposer. This reduces the number of assembly steps making it more cost-efficient. The 3D PolyBoard requires more fabrication steps than 2D PolyBoard, as the same lithography steps are repeated to fabricate the waveguides in each layer, however it compensates with unique structures and functionality. MCF pigtails were edge-coupled at the Tx and Rx outputs, by means of a fiber array where the MCFs had been positioned and properly rotated prior to assembly.

## V. CONCLUSIONS

Hybrid photonic integration concepts from the TERIPHIC and POETICS projects, that utilize a polymer PIC motherboard hosting InP optoelectronic components, have been presented. Using the same fundamental building blocks, terabit optical engines can be realized with WDM and SDM functionality, that are suitable for the next generation optical transceivers within the DCs. Terabit WDM and SDM optical engines realized within these projects have been shown. The waveguide interfaces are the same among the EMLs, PDs and PolyBoard waveguides, meaning that the coupling interfaces can be optimized once, achieving efficient coupling and repeatable behavior. This versatility in functionality is enabled from the wide PolyBoard toolbox and the established InP EML and PD technology at Fraunhofer-HHI.

## ACKNOWLEDGMENT

This work was supported by Horizon2020 projects TERIPHIC (G.A. nr. 825502) and POETICS (G.A. nr. 871769)

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