# High Speed Transceivers beyond 1.6Tb/s for Data Centre Networks

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**Abstract** *The demand for compute capacity is currently doubling every 3.4months. This has accelerated the need for Terabit optical transceivers for data centre applications. Scaling options, and photonic and electronic technologies that can meet such demand are presented. ©2023 The Author(s)*

## The accelerating need for compute and connectivity in the data centre

The recent introduction of generative and large-language AI models of which ChatGPT is currently the most famous example is not only creating waves in general society but also in the domain of the hardware underlying its operation. As shown in Fig. 1, the demand for compute capacity is currently doubling every 3.4months, driven solely by the training needs of such AI [1]. Even though it is difficult to imagine such growth to continue over the next couple of years, its impact on the demand for more capacity on short-reach optical interconnect inside data centres is already clear: a rapid introduction of 200G/lane solutions has now started, faster than originally anticipated. Relying on both 100G/lane and 200G/lane technology, industry is now targeting pluggable and co-packaged optical transceivers with multiple Terabit/s capacities [2]. This paper discusses options to scale towards Terabit/s transceivers, from a system and technology point of view.

## Transceiver scaling options

Assuming that such growth in demand for compute and associated interconnect continues for at least some time, the question is then obviously how do we go from today's 200G/lane technology to Terabit/s capacities? Looking back at 25G/lane technology which was used to realize 100G optical transceivers constructed from 4 such lanes, different steps can be distinguished on the route to today's 800G capable transceivers. Industry took a first major step by doubling the spectral efficiency to 50G/lane through ~25Gbaud 4-level pulse amplitude modulation (PAM-4). This allowed to realize 200G optical transceivers relying on essentially the same optics and electronics processes as the 25G/lane devices. Significant effort was required

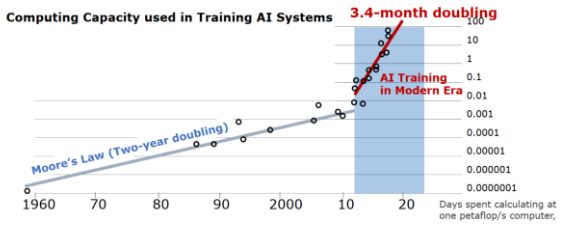


**Fig. 1:** Compute capacity for training AI systems [1].

to realize linear opto-electronic front-ends and PAM-4 capable SerDes (mixed-signal or DSP-based) with a power consumption and physical size that fits pluggable modules, but no new process development was necessary. Further leveraging the same photonic and electronic processes, in a next step the number of lanes was increased from 4 to 8, thus realizing 400G transceivers. However, doubling the number of lanes does not gain one much in terms of energy efficiency (pJ/bit) nor frontplate density on the switches, and reduces production yield. This explains the move towards 100G/lane (~53Gbaud PAM-4) technology relying on new photonic and electronic processes, from which again 4-lane 400G optical transceivers were built. This repeated itself with the recent introduction of 800G modules, and currently we are at the stage of 200G/lane (~106Gbaud PAM-4) technology.

With 1.6T and 3.2T firmly on the roadmaps, the same evolution may repeat itself: the first 1.6T transceivers will use an 8-lane, 200G/lane approach. In a next step, new photonic and electronic processes with EO/OE (electro-optic) bandwidths of at least 100GHz will be required for new 400G/lane technology. Clearly, there will be significant challenges: silicon photonics, which is currently one of the workhorses in this market, struggles with modulators that have electro-optic bandwidths as high as 100GHz, and will require heterogeneous integration to support

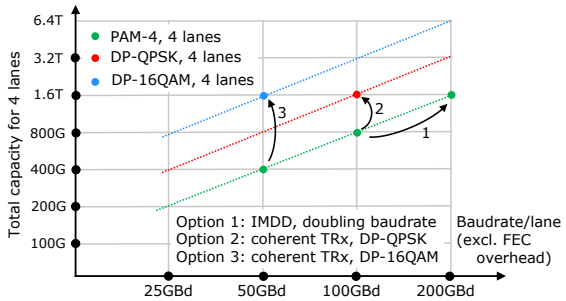


**Fig. 2:** Scaling options to 400G/lane capacity, 4 lanes make a 1.6T transceiver.

this. Electro-optic integration with focus on achieving >100GHz bandwidth throughout the front-end optical engine (including the connections between photonic and electronics ICs) will be a significant hurdle to overcome.

An alternative (see Fig. 2) could be to use more advanced modulation formats to further increase the capacity per lane while relying on existing 200G/lane (100Gbaud PAM-4, >50GHz EO bandwidth) photonics and electronics. A first option is ~100Gbaud (the exact baudrate depends on the selected error correcting code) dual-polarization quadrature phase shift keying (DP-QPSK) which allows 400G/lane capacity relying on coherent technology. Another option is ~50Gbaud (same remark as before) DP-16QAM, leveraging existing 400ZR technology with simplified DSP (dependent on selected wavelength band and target fibre reach). Optical functionality such as polarization splitting/ combining, and optical hybrids are required but these can be readily integrated into the PIC with marginal additional cost. With the power and density for coherent and IMDD DSP converging [3], the differential to move to coherent technology then mainly originates from the need for a laser with improved linewidth (e.g. <500kHz) to provide the local oscillator. Dependent on the system-level implementation, either a single higher power laser (whose output is split between the transmitter and the local oscillator) or two lasers per module can be used. An alternative which avoids such additional laser are interferometric detection schemes.

It is interesting to compare these different options from an optical budget point-of-view. Fig. 3 shows achievable optical budgets under the simplifying assumptions that sufficient electro-optic bandwidth is available in the components such that impact of intersymbol interference is negligible, the reach and wavelength is such that the penalty due to chromatic dispersion is negligible and the linewidth of the lasers is small enough that resulting penalty is negligible. This optical budget therefore provides a best-case

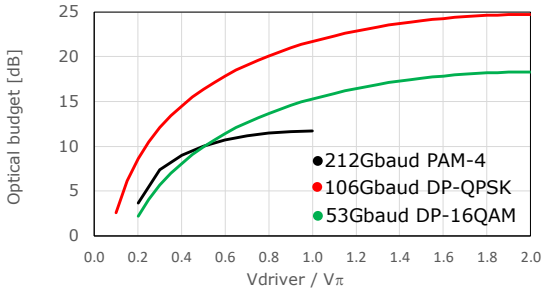


**Fig. 3:** Optical budget as a function of relative drive voltage for different 400G/lane scaling options (laser power: +10dBm, laser RIN: -145dB/Hz, modulator excess loss: 4dB (2dB extra loss for polarization combiner), photodetector responsivity: 0.7A/W, input-referred noise density receiver: 20pA/Hz$^{1/2}$, receiver bandwidth: 60% of baudrate, hybrid loss: 10dB incl. polarization splitting, coherent receiver common-mode rejection: 20dB, laser coherent transceiver 50/50 split between DP-IQ modulator and local oscillator, target bit-error rate: 2x10$^{-4}$).

baseline. For low drive voltages (lowest energy consumption for the driver electronics) up till 0.5x$V_\pi$ (halfwave voltage), PAM-4 modulation slightly outperforms DP-16QAM, mainly due to the high loss of the modulator in the coherent case. Above 0.5x$V_\pi$, the loss of the modulator for the DP-16QAM case becomes sufficiently low such that the sensitivity gain due to mixing with the local oscillator outperforms PAM-4. DP-QPSK gives best performance irrespective of the modulator drive voltage, which is mainly due to its fundamental sensitivity advantage. If no transmit-side equalization is necessary, DP-QPSK has the further advantage that no linear drive electronics would be required, simplifying the overall transmitter and reducing its power consumption. The picture painted here will change depending on the amount of chromatic dispersion and bandwidth limitations in the transceiver components, and the sophistication of DSP equalization to overcome these. Clearly, ~100Gbaud DP-QPSK can be an interesting option for future 400G/lane transceivers.

**Optics for 400G/lane transceivers**

Opto-electronic front-end bandwidths around ~50GHz will be required to support ~100Gbaud DP-QPSK, dependent on the used DSP. InP processes have demonstrated integration of modulators and detectors with sufficient bandwidth [4]. Silicon photonics with its higher integration density and manufacturing throughput can integrate both photodetectors (e.g. Ge devices) and various modulators that are suitable. Mach-Zehnder modulators face trade-offs between insertion loss and bandwidth versus required drive voltage, although these can be broken to some extent through the use of e.g.

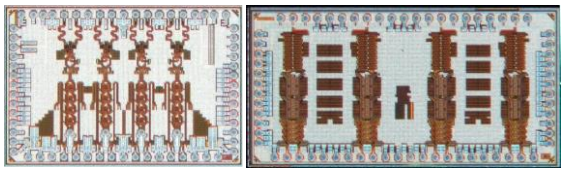

**Fig. 2:** >100Gbaud capable SiGe BiCMOS modulator driver (left) and >100Gbaud capable SiGe BiCMOS transimpedance amplifier (right), traveling wave structure are visible.

optical equalization [5]. Electro-absorption modulators (EAMs) with >50GHz bandwidths have been demonstrated [6]. Franz-Keldysh EAMs integrated in silicon photonics can only be used in the C-band, however recently progress is being made in the integration of quantum-confined stark-effect (QCSE) EAMs suitable for the O-band [7]. A silicon photonic IQ transmitter relying on EAMs was demonstrated in [8].

If coherent transceivers were to be deployed inside data centres, they will likely need to be manufactured at significantly higher volumes compared to today's telecom market. Integration of low linewidth lasers on the coherent PIC can then be an appealing proposition. Different integration techniques are currently being developed at imec such as flip-chip bonding and micro-transfer printing [9]. In addition, integrated wavelength locker circuits to tune the local oscillator laser to within a few GHz of the incoming modulated wavelength are crucial: research is currently on-going at imec to integrate such functionality directly on the silicon PIC.

Supporting ~200Gbaud PAM-4 will require a doubling of the electro-optic bandwidth to ~100GHz. Thin-film LiNbO3 integrated on silicon photonics then becomes a promising option [10]. At the detector side, III-V uni-traveling carrier (UTC) photodetectors can be integrated. Imec is making progress to heterogeneously integrate thin-film LiNbO3 modulators and UTC photodetectors (with bandwidth >150GHz) on their silicon photonic platforms, relying on micro-transfer printing [11-13].

**Electronics for 400G/lane transceivers**

To support ~100Gbaud operation, also the electronic front-ends (modulator driver, transimpedance amplifier, front-ends of analog-to-digital (ADC) and digital-to-analog (DAC)) should ideally have ~50GHz bandwidth: the actual requirement depend on the used equalization. In most cases, the front-end electronics need to be linear to support multilevel modulation and/or equalization. One way to achieve sufficient linearity, bandwidth, output voltage swing (in the case of the modulator driver), low-noise operation and gain (in the case of the transimpedance amplifier) is to use traveling-wave amplifiers. Previously 100Gbaud front-electronics used InP heterojunction bipolar transistor (HBT) processes [14]. Recently imec has been working towards SiGe BiCMOS circuits that meet the specifications for >100Gbaud operation. The use of SiGe BiCMOS not only allows for a higher manufacturing throughput and lower cost, but also allows to include features such as digital reconfigurability of gain, peaking (e.g. continuous-time linear equalizers) and bandwidth settings. Fig. 4 shows a four-channel modulator driver designed and fabricated using 55nm SiGe BiCMOS, featuring >70GHz bandwidth and a linear differential output voltage swing of at least 3.5Vpp (total harmonic distortion for a 1GHz tone less than 2%). The four-channel linear transimpedance amplifier has a bandwidth of ~62GHz with up to 76.8dBΩ gain.

A critical part of many optical transceivers are the ADCs and DACs. These enable DSP, which is necessary to overcome distortion introduced by the transmission channel, and perform data recovery which in the case of a coherent receiver consists of polarization rotation and demultiplexing, IQ and skew imbalance correction, symbol estimation, optical carrier phase & frequency estimation, and error correction. Operation beyond 100Gbaud requires ADC and DAC sampling rates far beyond 100GSamples/s, with typical resolution 7 to 8bit and 4 to 5 bit ENOB in the high-frequency band to support DP-16QAM. In a first attempt to achieve such sampling rates, an analog interleaver was realized using a 55nm SiGe BiCMOS process that allowed interleaving of the outputs of sub-rate DACs, thus shifting the ultra-high-bandwidth functionality from the CMOS DSP chip to a SiGe BiCMOS chip [15]: 100Gbaud PAM-4 was demonstrated. Recently, imec has started to address bottlenecks in achievable analog bandwidth of conventional wireline ADC and DAC architectures fully integrated on CMOS. Novel approaches for both ADC and DAC are currently being implemented using a 5nm FinFET CMOS process, which hold the promise of a significant reduced power consumption compared to the state of the art. Implementation using 3nm CMOS is being planned.

**Conclusion**

Different options to scale to 400G/lane were provided. Photonic and electronic technologies being developed towards ultra-high-baudrate optical transceivers have been highlighted.

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